

LEARNING ABOUT LOGIC by P.J. Horwood, G3FRB*

Part 1. Introduction

THE purpose of these articles is not to explain how integrated circuits are made and how they work, but how to use them.

Currently, the commonest and cheapest ics are known as ttl, meaning the basic gate configuration is based on a multi-emitter transistor rather than resistors and transistors (rtl) or diodes and transistors (dtl). However, what follows is equally applicable to all types, and no further mention of the various types will be made until much later in this series when speed of operation and power consumption will be dealt with.

Most textbooks, after dealing with the basic functions of ics, proceed towards their incorporation in calculators and computers, whereas the radio communication technician is much more interested in counters, frequency dividers and frequency synthesizers. It is the intention of this series to take the reader by easy stages to the use of ics in the divide-by-N phase-locked-loop synthesizer.

It is not necessary to consider the physics of transistor action to employ them, neither is it necessary to consider the transistors in an integrated circuit to use it. In fact, it is positively disadvantageous to the initial understanding of logic circuits to get involved in the interior detail of a device which cannot be adjusted or repaired. Later, the reader can find information about loading (fan-out), open collectors, etc in any manufacturer's manual.

Gates

The logic function of the various gates can be explained by similes with simple dc circuits. Consider the circuit of Fig 1. It is obvious the lamp will be lit only when both switches A and B are closed. If either or both are off, the lamp will be out. This illustrates the function of the AND gate.

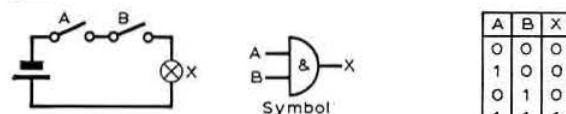


Fig 1.

Fig 1 also includes a simple way of showing all the combinations of A, B and X without a lengthy description; this is called a truth-table. The conditions are shown in binary form; a switch is either open (0) or closed (1). Likewise, the lamp is either off (0) or on (1).

A special kind of algebra, known as Boolean algebra, together with binary arithmetic is used in logic circuits and calculations, and a limited amount will be employed in these articles and will be explained as it arises. One should not be put off by this, as it requires simple logical thought! It is interesting to note that Boolean algebra was invented by George Boole early in the last century to solve complex logic problems long before electronics as known today came about.

A few words about binary arithmetic; it is a very simple system based on powers of two, rather than powers of 10 in the decimal system. Only two numbers are used, 0 and 1, whereas there are 10 values 0 to 9 in the latter.

Because of familiarity with the decimal system one does not stop to think that a number such as 247 is made up of successive powers of 10. It could be written as $(7 \times 10^0) + (4 \times 10^1) + (2 \times 10^2)$. This of course equals $7 + 40 + 200$; 247. If the concept of 10^0 is puzzling it must be explained that any number to the power zero equals 1.

In the same way, a binary number is made up of successive powers of 2. Listed below are some powers of two with their decimal equivalents. The range is infinite and further powers can be generated simply by doubling.

Binary	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰
Decimal	64	32	16	8	4	2	1

Later, when counting circuits are described, the convenience of the binary system will become fully apparent.

The next type of gate can be illustrated by Fig 2. Here the lamp will be lit if A or B or both are closed. It illustrates the action of an OR gate.

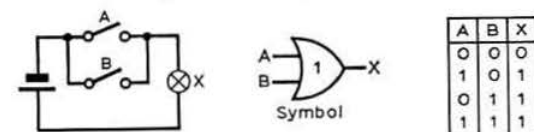


Fig 2.

A further gate can be understood without a simile; it is known as an inverter, or NOT (Fig 3). The convention of writing a bar over a number to indicate its complement will be seen; read as NOT A, or A BAR.

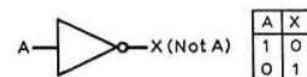


Fig 3.

Finally, to the last of the main family of gates, the NAND and NOR.

These are combinations of AND and NOT, and OR and NOT (Figs 4 and 5).

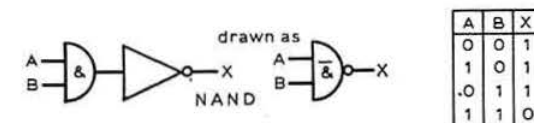


Fig 4.

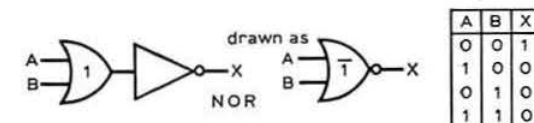


Fig 5.

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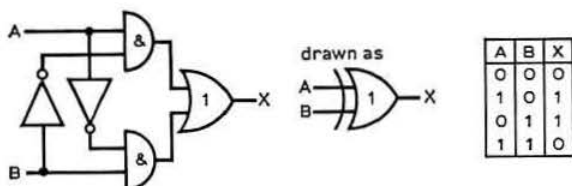


Fig 6.

Although we have seen the five basic gates, there is one further development of the OR gate which must be mentioned. The normal OR gate produces a 1 if either or both inputs are 1, but there is a need for a device which responds to either input but not to both. This is called an EXCLUSIVE OR. The truth table and the development from AND, OR and NOT gates is shown in Fig 6. The inputs to the AND gates must be either A and NOT B or B and NOT A for the output to change to 1.

In the foregoing descriptions the inputs to the various gates have been limited to two; in practice, ics are available with 2, 3, 4 or more inputs.

Flip-flops

All the devices so far described respond immediately to the application and removal of a stimulus; in other words, they possess no memory. Nevertheless, from them can be developed the flip-flop which has a rudimentary one. The flip-flop, not to be confused with the multivibrator, has two stable states to either of which it may be switched by a suitable input. Furthermore it remains in that state until another stimulus is received. Like the good soldier, it obeys the last order and remembers it.

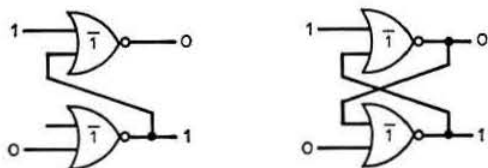


Fig 7.

Consider the diagrammatic sequence of Fig 7.

(a) If the upper input at present at 1 is removed, the output will not change because it is held at 0 by the output from the lower gate.

(b) Because the lower gate input is 0, the uncommitted input can be cross-connected to the upper gate output. There will be no change in the output states. Both inputs can be removed and each gate will be held in its present condition by the cross-connected output from the other gate. If the upper gate input is again made 1, or the lower gate input again made 0, still there will be no change. Only if the lower gate is made 1 will its output become 0; this will enable the upper gate output to become 1, being cross-connected to the lower gate it will hold that gate's output at 0 even if the lower input is removed. Both inputs can be removed because it has now flipped to the other self-perpetuating or stable state.

It can be seen there are two stable states, determined by whichever input was last made 1. It is known as a bistable, an alternative name for flip-flop.

The diagram is repeated in Fig 8 with new labels for

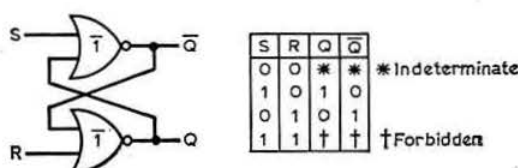


Fig 8.

inputs and outputs. The inputs are labelled SET and RESET, meaning a 1 can be set at the Q output by the application of a 1, and Q can be reset to 0 by the application of a 1 to the other input. Note that Q and $\bar{Q}$ are opposite in condition, or complementary. These are the conventional labels for flip-flop outputs. The notes beside the truth-table refer to the conditions marked with a star and a dagger. When a flip-flop is switched on without inputs it cannot be determined whether the Q or $\bar{Q}$ will become 1. The state is indeterminate. The last condition is forbidden because the states of Q and $\bar{Q}$ are in conflict.

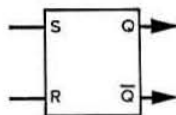


Fig 9.

The standard diagram for an SR flip-flop is shown in Fig 9. Note that the positions of Q and $\bar{Q}$ have been reversed to place Q opposite the SET input.

Part 2 of this series will deal with several more complex forms of flip-flop and will progress towards their utilization in counters and dividers. Subsequent parts will explain programming of the basic binary divider to make it divide by decimal numbers, and its use in the phase-locked-loop frequency synthesizer. □

CATALOGUES RECEIVED

Doram catalogue

A 12-page leaflet providing details of additions and alterations to the Doram Electronics catalogue is now available. In addition to price reductions (announced before the alteration in the 25 per cent VAT rate) there are a number of new lines. Of particular interest to radio amateurs is the inclusion of a range of modules, transverters and a frequency counter/prescaler manufactured by Microwave Modules.

Copies of the catalogue amendment leaflet can be obtained from Doram Electronics Ltd, PO Box TR8, Wellington Bridge Industrial Estate, Wellington Bridge, Leeds LS12 2UF; tel Leeds (0532) 34222.

Eagle International catalogue

The new Eagle International catalogue comprises 64 pages listing more than 500 different items of which more than 40 are new. A full-colour production, the catalogue is divided into nine sections, each covering a different product, eg hi-fi, audio, headphones, microphones, test equipment. It is available on request from Eagle International, Precision Centre, Heather Park Drive, Wembley, HA0 1SU. □

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Part 2. Flip-flop types

IN Part 1 the various gates were introduced, and from them the basic rs flip-flop was derived. Remember that the rs has two inputs, a high (1) applied to s making Q high, and a high applied to r making Q low, $\bar{Q}$ always being complementary to Q. A flip-flop can be much more useful if the r and s inputs are combined to form one trigger or clock input. Input pulses will cause r and s action alternately (Fig 10).

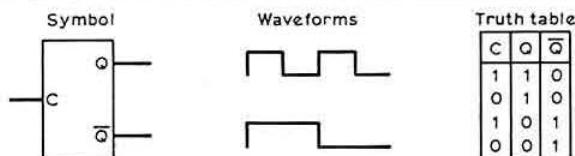


Fig 10. Top waveform C, lower Q

From the truth-table it can be seen that every time the clock input changes from 0 to 1 the Q and $\bar{Q}$ outputs exchange condition. This is called complementing. The waveforms illustrate this; notice the frequency has been halved. It is important to note that it is the leading edge of the input waveform which causes the output to change.

This simple flip-flop is not available as an ic package although it may be made up from a dual NOR gate. It does sometimes form part of more complex devices.

Development of integrated circuit technology lead to many variations of the basic flip-flop. To some extent these have been rationalized into the following types: D type, edge-triggered J-K, master-slave J-K.

D type (Fig 11)

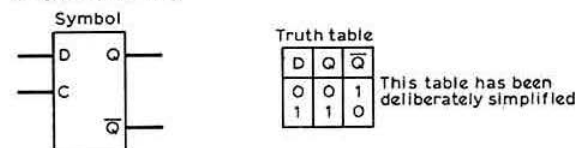


Fig 11.

The D input decides whether Q shall change to 1 at the next clock pulse; a 1 at D does not change the state of Q on its own. For Q to change, D must be held high before the clock pulse arrives and be maintained at that level for a specific period at least as long as the clock pulse. After this explanation it is possible to draw a truth table showing the whole action (Fig 12). This is not the normally accepted diagram for a D type but at this stage it is easier to understand. Pulses are shown at C; D is shown in the two possible conditions, as are the Q and $\bar{Q}$ states.

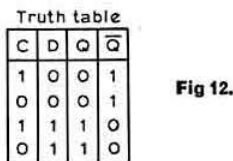


Fig 12.

However, the complexity of flip-flop packages is increasing and will continue to do so in subsequent types, and because of the increased usefulness of more complex devices the D type is less used on its own but is often used as a part of a more complex package.

Edge-triggered J-K (Fig 13)

Two new inputs, J and K, have been introduced and it is now necessary to explain the conventional way of displaying a truth table. The C input is not shown, only the effect on the outputs after each clock pulse has arrived (Fig 14). Present time is described as T_n , T_n+1 means after the next clock pulse and so on. $\bar{Q}$ state is always assumed to be complementary to Q.

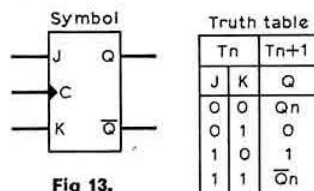


Fig 13.

Fig 14.

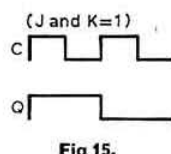


Fig 15.

When both J and K are low no change takes place at Q or $\bar{Q}$ even though a clock pulse arrives. If J is held high Q will go high at the next clock pulse, whereas if K is held high Q will become low at the next clock pulse. If both J and K are both held high permanently Q and $\bar{Q}$ will exchange states at every clock pulse. The change of state takes place at the leading (rising) edge of the input waveform (Fig 15).

The positive-edge triggered flip-flop is generally restricted in use to high speed circuits.

M-S-J-K flip-flop (Fig 16)

The name is derived from the internal circuit; this consists of a pair of flip-flops, the master driving the slave, usually exchanging function at each clock pulse.

The truth table is the same as that for the positive-edge triggered J-K but the change of state takes place at the negative edge of the clock pulse. Although this difference may seem of little consequence it has an important bearing on the way a group of flip-flops will count, as we shall see later.

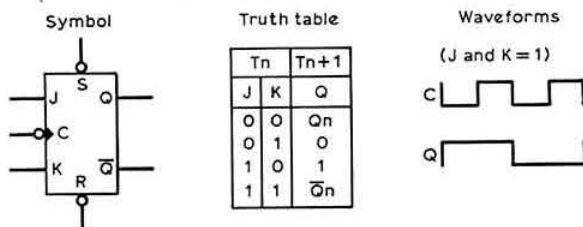


Fig 16.

On the symbol, inputs S and R have been restored. These have overriding control of the output states, irrespective of

(Continued on p505)

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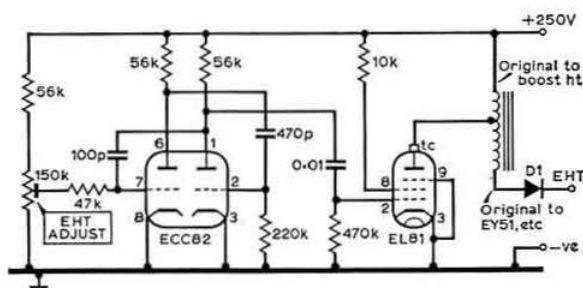


Fig 4. EHT generator

Component considerations

TAA350 may be replaced with a TAA350A, in this case the pin numbers are all rotated clockwise by three pins.

The lowpass filter in Fig 1a uses Philips cores H20; an equivalent is the Mullard LA1302. A slightly lossy substitute can be wound using LA1 cores; fill the formers with fine wire and then tune them in circuit to 900Hz, 2kHz and 3kHz respectively by removing turns and using an oscilloscope and audio generator.

The 1.3V voltage-dependent resistors in the bases of TR14 and TR24 may be replaced by two silicon diodes in series (BA100) or possibly with a 1.3V zener diode.

A suitable scan coil assembly and permanent magnets for focussing may be obtained from an old tv set having a tube neck of similar size to the 5FP7. The scan coils should have

Parts list

- L1, L3** Philips H core type H-20 or Mullard LA1302, 400 turns of 34 swg enamelled copper wire.
- L2** Philips H core type H-20 or Mullard LA1302, 550 turns 34 swg.
- L4** Horizontal deflection coil approximately 4.6Ω.
- L5** Vertical deflection coil approximately 38Ω.
- D1** BY140, BY176 or BY182.

their windings series or parallel connected as necessary to give the nearest resistance readings to those quoted in the parts list.

Mechanical design

The electronic and high-voltage circuits can be housed in a cabinet measuring 160mm wide by 240mm high by 300mm deep. However, it may be preferable to build the power supplies in a separate cabinet as trouble may be experienced with the ac fields surrounding the transformers.

The monitor tube is clamped against the front panel by fabricating a round clamp from a strip of 18swg aluminium, a pinch-bolt should be used for tightening onto the tube, and four lugs bent out at 90° to fix the clamp to the front panel.

The transistor stages may be mounted on two vector boards measuring 130mm by 220mm, or by using printed circuit boards. The input stages TR1 to TR12, TR21 and TR22 are mounted on one board with the sweep stages on the other. The boards are placed vertically on both sides of the monitor tube and fixed to small distance-spacers. □

Learning about logic

(Continued from p501)

the clock and J and K conditions. Only a pulse is required at S or R to set Q high or low. Sometimes the reset terminal (R) is called Clear (CL). A separate truth table shows the S and R action (Fig 17). Note S and R must be made low (0) to change the output state. This is signified by a circle on the leads. Similarly the clock input is designated negative-edge triggered by the circle and arrowhead respectively.

Truth table			
S	R	Q	$\bar{Q}$
0	1	1	0
1	0	0	1

Fig 17.

The M-S-J-K with set and clear is the most complex flip-flop and has the greatest number of potential uses. The reader may wonder at all this increasing complexity, but its purpose will become apparent when groups of flip-flops are used in various types of counter.

It is advisable to remember what the values 1 and 0 represent in terms of voltage. The blocks described here are all positive logic; 1 is always positive with regard to ground. The normal supply voltage (V_{cc}) for ICs is 5V, therefore 1 equals 5V or something approaching it; not less than about 3.5V. 0 equals zero volts, or a low voltage not exceeding about 1V. It is important to grasp that 0 does not mean open-circuit. In fact most logic inputs take up a high (1) value if left open. All inputs must be tied back to a definite logic level

if not used; either to a previous output terminal etc, or to ground (0) or V_{cc} (1) as the circuit demands. Two examples of this are shown in Fig 18.

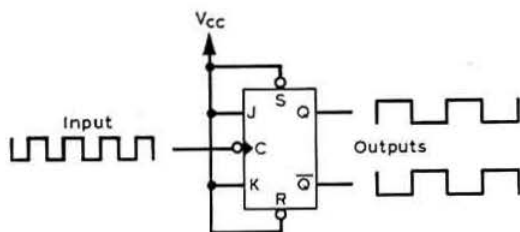


Fig 18.

The M-S-J-K is required to act as a divider, the Q output changing state at each input trailing (negative-going) edge. To allow this both J and K must be held permanently high. Although for experimental lash-ups it would be permissible to leave J and K open-circuit (and thus high), in a finalized circuit stray pick-up of fast pulses could upset the operation. Therefore J and K are strapped to V_{cc} . The S and R inputs are not required and to prevent possible spurious operation they are also held permanently high. This is a good example of how the most complex package is not necessarily fully exploited in some applications, yet for the sake of standardization similar ICs are used in each stage.

We have now reached the point where several flip-flops may be cascaded to form increasingly complex dividers or counters. These will be the subject of Part 3. □

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Part 3. Dividers and counters

The name "counter" is synonymous with the word "divider". A number of flip-flops may be connected to divide by some number, and if required, steps may be taken to display the total number of input pulses received, within the capacity of the divider.

Fig 19 shows four flip-flops cascaded, the unused inputs J, K, S and R, and output Q left unconnected to simplify the circuit. It forms what is called a binary up counter. Because there are four stages, the total capacity before resetting to zero is 2^4 (16). The conditions of terminals A, B, C and D will range from 0000 to 1111 (Decimal 15). There are 16 permissible states. The truth table ("a") shows that the conditions of A, B, C and D are the binary equivalent of the decimal input number. To use this circuit as a simple counter the output terminals could be made to light lamps. When lit the lamps would have the decimal values of 1, 2, 4 and 8 respectively. To further illustrate the division function the waveform diagram is also given (Fig 20). For a total of 16 input pulses (negative-going edges) there are eight at A, four at B, and so on.

In practice, each successive output would be displaced slightly to the right. This is due to what is known as propagation delay. Propagation delay is the time taken for an output to change after the input is applied. The time is very small, typically 50ns, but if they were driven by a high frequency, 50ns could become a significant part of the input pulse duration, and false counting could occur.

This leads to more complex dividers to extend the upper frequency of operation. In the above example the input is applied only to the first flip-flop, its output driving the second one, and so on. It is known as a ripple-through or asynchronous circuit. For higher frequency performance a synchronous circuit must be used, where all the clock inputs are driven simultaneously and gating employing the J and K inputs determines the count sequence. Even so, the simple four-stage ripple-through divider will operate at clock frequencies in excess of 10MHz with suitable ICs, but further cascaded flip-flops increase the propagation delay and limit the speed of operation. The delay is cumulative.

It has been shown that four stages have the ability to divide by 2^4 , therefore it can be said that N stages will divide by 2^N (N meaning any number). Because the flip-flop is a two-condition device a collection of them will divide by successive powers of two.

By various methods it is possible to modify the count sequence to cause a group of flip-flops to divide by some desired decimal number. For a given number of flip-flops it is only possible to modify the circuit to divide by a decimal

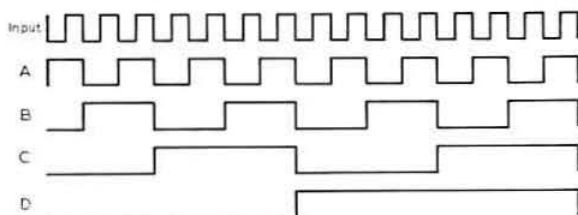


Fig 20.

number not exceeding the equivalent of the maximum binary capability. The four-stage divider may have its sequence altered to divide by any number up to 16. If it were necessary to divide by 60, for instance, the basic binary capability would have to be 64. This equals 2^6 , or six stages.

Let us consider various ways of modifying a count sequence, taking a maximum count of 10 as an example. Binary counters (dividers) modified to count to 10 are described by the term binary-coded decimal (bcd). The methods require the number of count conditions to be limited to 10, either by limiting the maximum number, commencing to count at three rather than zero, or by skipping some conditions in between.

The circuit in Fig 21 is what is called a skip counter. From the truth-table it can be seen the normal binary count sequence proceeds up to seven, at the eighth count DQ goes low, taking B and C stages S with it, modifying the count to $2 + 4 + 8$, a total of 14. The next count, although the ninth, is read as 15, and at the very next count all stages revert to zero. The capacitor is necessary to prevent Bs and Ds being held permanently low, otherwise the counter would lock up. A negative-going pulse via the capacitor is sufficient. The capacitor is non-critical, about 0.01μF being satisfactory. Note that the speed of the negative-going pulse from DQ is not related to the input frequency but to the speed of operation of the flip-flop.

To design a counter using this method it is necessary to subtract the new maximum count required from the maximum available, ($16 - 10 = 6$) and connect the feedback line to the appropriate set terminals.

Feedback to Aset = 1 skipped

" " Bset = 2 skipped

" " Cset = 4 skipped

Any required combination may be connected in parallel.

The speed of the skip-counter is limited because it is asynchronous, as previously explained, and further by the time taken for the set inputs to respond to the pulsed low

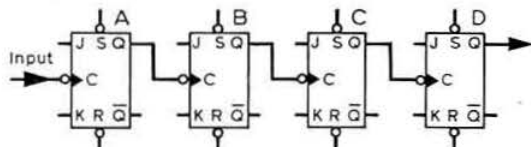


Fig 19.

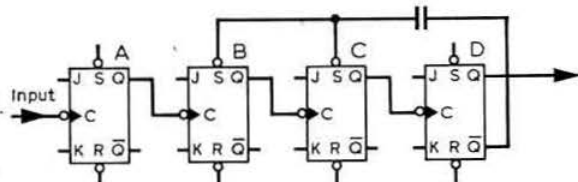


Fig 21.

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TRUTH TABLES

a	b	c	d
Input	Input	Input	Input
0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0
1 0 0 0 1	1 0 0 0 1	1 0 0 0 1	1 0 0 0 1
2 0 0 1 0	2 0 0 1 0	2 0 0 1 0	2 0 0 1 0
3 0 0 1 1	3 0 0 1 1	3 0 0 1 1	3 0 0 1 1
4 0 1 0 0	4 0 1 0 0	4 0 1 0 0	4 0 1 0 0
5 0 1 0 1	5 0 1 0 1	5 0 1 0 1	5 0 1 0 1
6 0 1 1 0	6 0 1 1 0	6 0 1 1 0	6 0 1 1 0
7 0 1 1 1	7 0 1 1 1	7 0 1 1 1	7 0 1 1 1
8 1 0 0 0	8 1 0 0 0	8 1 0 0 0	8 1 0 0 0
9 1 0 0 1	9 1 0 0 1	9 1 0 0 1	9 1 0 0 1
10 1 0 1 0	10 1 0 1 0		
11 1 0 1 1			
12 1 1 0 0			
13 1 1 0 1			
14 1 1 1 0			
15 1 1 1 1			

"a" relates to Figs 19, 24;
"b" to Fig 22; "c" to Fig 21,
and "d" to Figs 23 and 25.

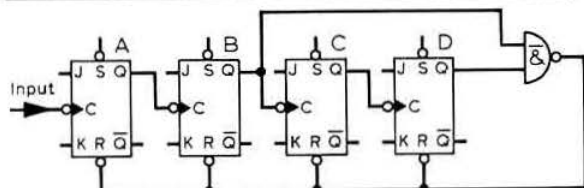


Fig 22.

signal. Even so, such a circuit is satisfactory up to several megacycles with normal tti integrated circuits.

Fig 22 shows a gated end-stop counter. The NAND gate detects one number greater than the desired count (in this case 10) and uses the resultant low to reset all stages back to zero. As a method it has limitations; a forbidden state (10) momentarily occurs, and because the reset signal also effectively removes the 10-state the tenth pulse is extremely short.

If such a counter were used at relatively low frequencies the extra state could be ignored, but if it were followed by a logic stage the speed of operation of it could well be fast enough to respond to the spurious pulse. Surprisingly such a circuit can be used at high frequencies where the duration of the reset pulse is significant in relation to the normal input pulses. Then the ninth count is gated (gate inputs from AQ and DQ), and reset to zero occurs very shortly afterwards.

The two previous examples exploit the S and R functions, the next example uses the J and K inputs and operates in an entirely different way (Fig 23). This is an asynchronous J-K-steered bcd counter. The truth table shows that flip-flop A changes state at each input pulse. B changes state at every other input but is prevented from changing at counts above eight because its J and K are held low by DQ once eight is reached. Flip-flop C changes state at every fourth count but is also prevented from changing above eight because it receives no drive once B is inhibited. Flip-flop D, although its clock is driven in parallel with B, is inhibited until a total count of seven is reached, when its J is made high via the AND gate driven from BQ and CQ. The next pulse above nine causes all stages to return to zero.

The author hopes this method of explaining counting stage by stage can be followed without too much difficulty; there is no doubt that the practical approach is easier to assimilate using such aids as the logic tutor reviewed in *Radio Communication* March 1975.

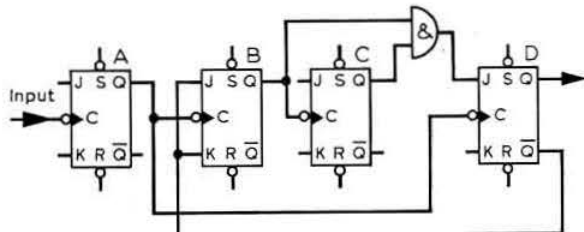


Fig 23.

The synchronous counter

All the previous examples have been based on the asynchronous counter, the frequency of operation being limited by accumulative propagation delays. Fig 24 shows a synchronous binary circuit; it can be seen that all the clock inputs are connected in parallel. Although all the flip-flops do not necessarily change at each clock pulse, when they are called upon to change they do so in synchronism, thus only one propagation delay occurs. The truth table shows that B changes after A becomes high, C changes after A and B become high, and D changes after A, B and C become high. This is achieved by the appropriate AND gates enabling the J and K terminals. One common type of ic is used, with integral AND gates, even in stages where the gate is not required. This is normal practice and also helps to ensure that the propagation delay is similar for each stage. The waveforms would be as shown in Fig 20, with only one propagation delay occurring between the input signal and all the outputs.

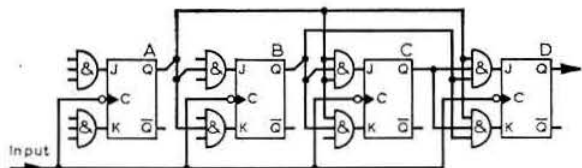


Fig 24.

Having introduced the synchronous concept in a binary counter, we can see in Fig 25 a synchronous bcd counter. AND gates dictate the sequence of counting as before, the upper limit (9) being determined by the connection of DQ to BJ. Once DQ has gone low at the count of eight, B and C stages are inhibited from changing and only A can change to make nine. At the tenth input A goes low, B and C are already low, and D goes low because its K is initially held high by AQ.

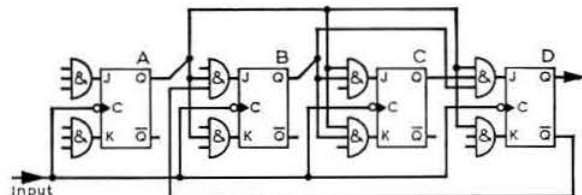


Fig 25.

We have now reached our goal of a synchronous bcd counter. The next article will deal with methods of modifying its count to make a fully variable counter. □

LEARNING ABOUT LOGIC by P.J. Horwood, G3FRB*

Part 4. Dividers and counters (2)

Before continuing with the further development of the variable divider and its use, the author wishes to explain the philosophy behind this series of articles.

To give some purpose to our consideration of logic circuits, it was decided to use the phase-locked-loop frequency synthesizer as the ultimate goal; it could equally well have been, for example, the frequency counter. The author hopes that when the series is complete he will have generated enough comprehension and interest in those with no foreknowledge to encourage further study of the enormous subject loosely called logic circuitry.

It is for this reason, as the more experienced will have noticed, that no mention has been made of other uses of the flip-flop, such as the ring and Johnson counter, and the shift register.

It was not intended to write a treatise covering the whole field, this would probably demand an article a month almost indefinitely. Such a series is in fact appearing currently in a contemporary of this journal.

The variable divider (counter)

At the end of Part 3 we arrived at the synchronous bcd circuit, various methods of modifying the count sequence having been shown. In theory it would be possible to develop a fully variable divider from any of the methods but in some cases the switching problems would be impractical.

The method most often used is related to the skip counter illustrated in Part 3, but instead of skipping a number of counts part way through the sequence the count is shortened by commencing to count from some number greater than 0. For example, if a bcd counter were to commence at 3 then only seven counts would take place. This process is called pre-loading.

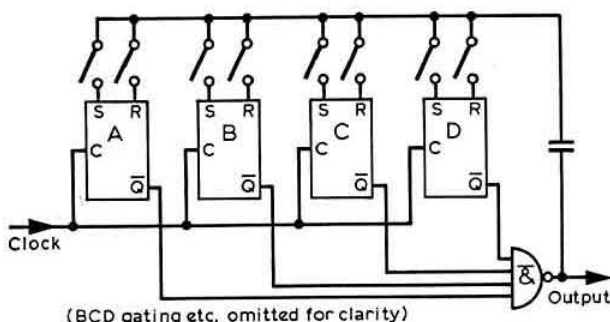


Fig 26.

Preload	D	C	B	A	Count
0	0	0	0	0	10
1	0	0	0	1	9
2	0	0	1	0	8
3	0	0	1	1	7
4	0	1	0	0	6
5	0	1	0	1	5
6	0	1	1	0	4
7	0	1	1	1	3
8	1	0	0	0	2
9	1	0	0	1	1

Fig 27.

* 14 Main Road, Hextable, Swanley, Kent.

Fig 26 shows the basic bcd synchronous divider with an additional NAND gate. The gate has inputs from A $\bar{Q}$, B $\bar{Q}$, C $\bar{Q}$ and D $\bar{Q}$; this is equal to 10. These inputs go high at the tenth trailing edge of the clock. The gate output goes low and via the coupling capacitor passes a low pulse to the appropriate set and reset inputs. The switching is shown using separate make and break switches; in practice a wafer switch designed to give a bcd output on four pairs of lines (four set, four reset) with 10 positions would be used. It is important that at the time of pre-loading, all the flip-flops are set to 1 or reset to 0 as appropriate for the particular preloaded number. Fig 27 gives the shortened count for each pre-loaded number.

Cascading dividers

So far we have examined only one variable decade divider. We shall see in the next article how this would allow 10 increments of frequency in a phase-locked-loop frequency synthesizer; for instance, a range of 1 to 10MHz. If we wished to provide increments of 100kHz, 10kHz and 1kHz, further dividers would be required. However, we will restrict the description to two cascaded dividers.

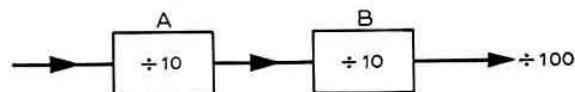


Fig 28.

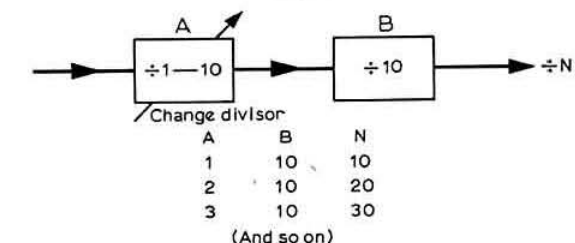


Fig 29.

If two dividers are connected in series (Fig 28), the resultant divisor is the product of the two individual divisors. While both these divisors are fixed, in Fig 29 one is made variable, 1-10. It is apparent it does not matter whether A or B is variable; N being the product. However, in practice it is more likely A will be fixed, becoming what is called a pre-scaler, reducing the input frequency to B by 10, and thereby making the inevitable self-capacitances etc of the switching associated with variable dividers less critical and allowing cheaper ICs to be used.

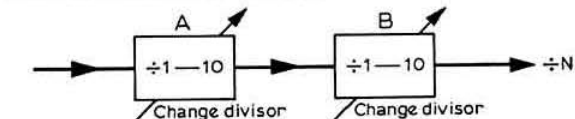


Fig 30.

The last example of simple cascading is given in Fig 30. N is the product of any number A 1—10 multiplied by any number B 1—10. For example, if A = 7 and B = 4, N = (divide by) 28. This arrangement, although giving variable division from 1—100 is not very convenient, as A and B do not have a distinct tens and units relationship. Take the previous example:

A	B	N
7	4	28

Whereas with a tens and units relationship, A being units and B tens:

B	A	N
4	7	47

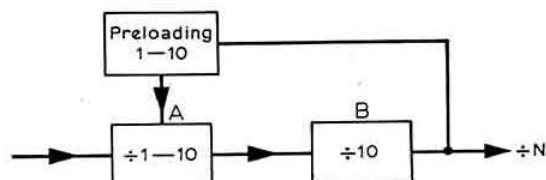


Fig 31.

A counts ten times									
4	10	10	10	10	10	10	10	10	10
1	2	3	4	5	6	7	8	9	10
B counts to ten									
B	A	N							
9	4	94							

Fig 32.

To achieve this it is necessary to extend the preloading principle (Fig 31). Divider A is preloaded every time B reaches 10; thus although A divides 10 times before this, the first time only it counts from whatever number was preloaded and on up to 10, all subsequent counts being 10. It could be called a "First-time-round" process. The variable count preloaded into A (for example, in Fig 32, six), will decide the first time round count, all other counts being 10. Therefore the variation 91-100 will be available in steps of 1.

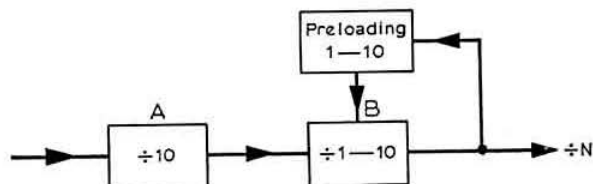


Fig 33.

A counts seven times						
10	10	10	10	10	10	10
1	2	3	4	5	6	7
B counts to seven						
B	A	N				
7	10	70				

Fig 34.

If the preloading was applied to B (Fig 33) each time B becomes full (reaches 10) a number will be preloaded into B. For example, in Fig 34 B was preloaded with three and therefore counts seven times. The total variation available is 10-100 in steps of 10.

Having shown preloading applied to A or B it is now necessary to consider preloading applied to A and B. The two

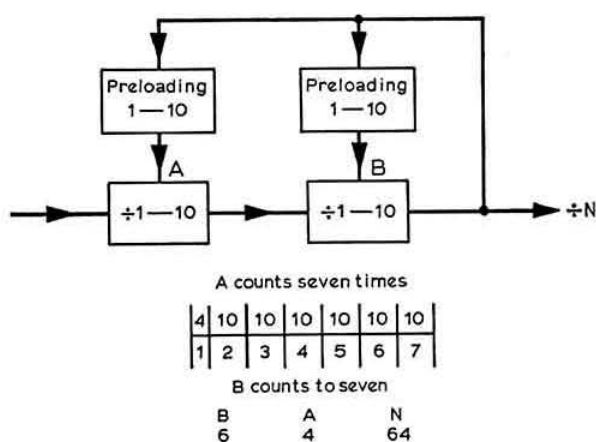


Fig 35.

previous examples have been combined in Fig 35. As an example, A is preloaded with 6 and counts to four the first time round, B is preloaded with 3 and therefore counts seven times, the first count being shortened as A only counts to 4. The total variation available is 1—100.

This article has been devoted almost entirely to logic circuit design; next month's article will deal with the embodiment of the variable divider in the phase-locked-loop synthesizer. □

CATALOGUES RECEIVED

Doram Electronics

The third edition of the Doram Electronics catalogue was available at the recent Radcomex 76 exhibition and provides up-to-date details of the many items now obtainable. Some prices have been reduced and special terms are now available to clubs and approved groups of amateur constructors. Of particular interest are the first two of a new range of mobile antennas for the range 130-174MHz. These comprise a $\frac{1}{2}\lambda$ unit with a loading coil and a $\frac{1}{4}\lambda$ antenna.

The catalogue is a quality production, freely illustrated and invaluable to any constructor. The cost is 60p, obtainable from Doram Electronics Ltd, PO Box TR8, Wellington Road Industrial Estate, Wellington Bridge, Leeds LS12 2UF.

Ferranti guides and price list

Three new semiconductor publications are now available from the Electronic Components Division of Ferranti Ltd. They are an E-line plastic transistor product guide, a metal can transistor product guide, and a discrete components price list. The two 20-page product guides give comprehensive details on a wide range of npn and pnp transistors, together with product indexing and cross-references. The discrete components price list is indexed alpha-numerically and covers in detail the available range of Ferranti semiconductors.

Further information on these publications may be obtained from Ferranti Ltd, Electronic Components Division, Gem Mill, Chadderton, Oldham OL9 8NP.

LEARNING ABOUT LOGIC by P.J. Horwood, G3FRB*

Part 5. PLL frequency synthesizer (1)

Before passing to a description of the phase-locked-loop frequency synthesizer, a little revision, or rather a fulfilment of an earlier promise (Part 2).

Positive edge triggering and the count sequence

It will be remembered that the M-S-J-K flip-flop was defined as negative-edge triggering while the basic J-K was said to be positive-edge triggered. Fig 36 shows a simplified ripple-through binary counter using the latter devices. The circuit is identical with that for M-S-J-Ks but the truth-table is not.

The first input does in fact ripple right through, putting all the Qs to 1, and each succeeding change from 0 to 1 at AQ causes flip-flop B to complement. This, of course, applies to all the other Qs when they go high. It is obvious that the count is downwards. A little thought indicates that if the interstage connections were made from $\bar{Q}$ to clock, the count would be upward, and conversely, if a negative-edge triggered group of flip-flops were connected $\bar{Q}$ to clock it would count downwards.

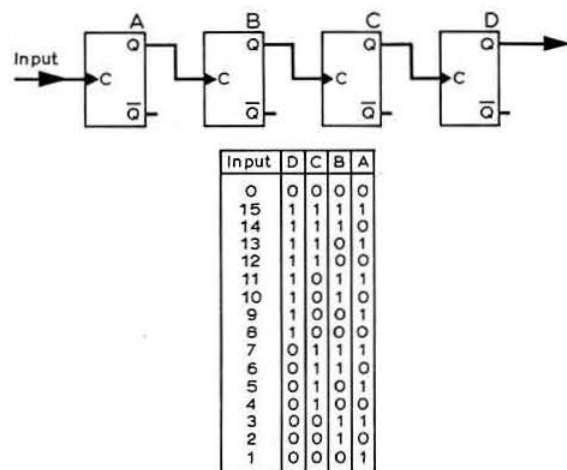


Fig 36.

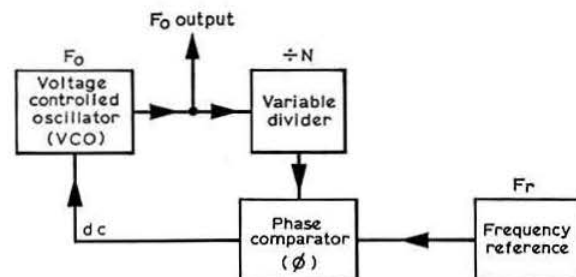


Fig 37.

The phase-locked-loop frequency synthesizer

Fig 37 shows the basic block diagram. The voltage-controlled oscillator is a conventional LC oscillator but also has a voltage-variable capacitor in parallel with the tuned circuit. Its output is required to do useful work, such as driving a mixer in a receiver or an exciter. The variable divider is now familiar. A source of high-stability oscillations is provided by the frequency reference. For the moment, the phase comparator will be considered as a device which receives two input signals and produces a dc output dependent on their difference.

This dc is applied to the varicap diode which alters the frequency of the vco. As an example, let the vco frequency F_0 be 10MHz, the division N be 10, and the frequency reference F_r be 1MHz. Then $F_0 = NF_r$, and, of course, $F_r = F_0/N$ and $N = F_0/F_r$. In this condition the dc output of the phase-comparator will be steady and hold the vco on 10MHz. Suppose the divider is changed to 9, then as F_r is constant the other input to the phase-comparator will be 10MHz divided by 9, and the dc output will change. In this example, the dc voltage must fall (as we shall see shortly) the varicap capacity will increase, and the vco frequency will decrease until it reaches 9MHz, when a stable condition or phase-lock is re-established. So it can be seen that the vco frequency is changed by altering the division ratio of the variable divider.

Now we must understand the operation of the varicap diode and the phase-comparator.

The varicap diode

Although during the series internal detail of ICs have been deliberately ignored, it is necessary briefly to consider the physics of a diode in order to understand its ability to become a variable capacitor. This ability is inherent in all junction diodes, but varicap diodes are specially designed to have predictable ranges of C commensurate with reasonable levels of Q . Fig 38 shows the three basic conditions of a diode, unbiased, forward biased, and reverse biased.

In (a) the N region is shown as predominantly negative, having an excess of electrons, while the P region is predominantly positive, having an excess of holes. The junction region is shown as having no charge and is analogous to the dielectric of a capacitor. If a diode were measured on a bridge it would be found to have significant capacity, as much as 100pF, depending on the construction. In fact, power diodes may have considerably greater capacity.

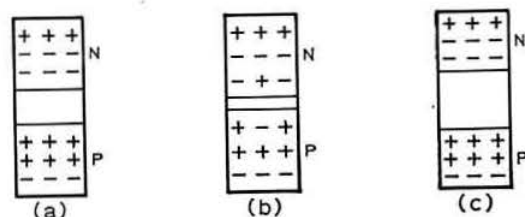


Fig 38.

* 14 Main Road, Hextable, Swanley, Kent.

Diagram (b) shows the diode forward biased, a current is formed by electrons and holes crossing the junction region. Reverse bias in (c) causes the electrons and holes to be drawn back to opposite ends, the junction region is increased in width and therefore the effective C is reduced. The varicap can be seen to be a device whose capacity can be made to change by an applied voltage. If this voltage were to be alternating, C would change in sympathy and cause frequency modulation if applied to a self-excited oscillator. However, in the phase-locked-loop frequency synthesizer, frequency modulation is highly undesirable and later we shall see how a low-pass filter is needed to prevent it.

The phase comparator

Two frequencies could be identical and yet have a phase difference. It is this phase difference which is detected and used to generate a dc voltage which itself is used to control an oscillator frequency via a varicap diode.

It is necessary to reintroduce a gate mentioned in Part 1, the exclusive OR. To save readers the need to refer back, the symbol and truth-table are repeated in Fig 39.

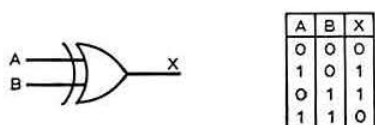


Fig 39.

Now let us consider two 1:1 mark/space ratio square waves applied to A and B. Fig 40 shows that when both signals are in phase the output is permanently low. (A and B = 0), whereas when 180° out of phase the output is permanently high. (A or B = 1). Note carefully that a phase difference of 90° produces a 1:1 mark/space ratio wave at twice the input frequency.

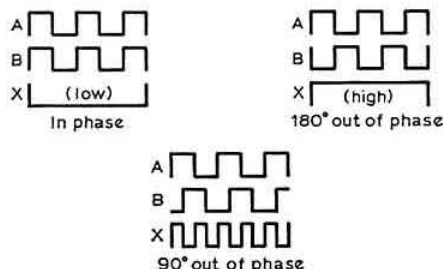


Fig 40.

Similarly, if the phase difference is less than 90° , the mark/space ratio will be less than 1:1, and when greater than 90° the mark/space ratio will be greater than 1:1.

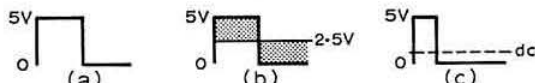


Fig 41.

What is the purpose of all this? Consider Fig 41 (a).

A single square wave of 1:1 ratio with voltage limits of 0 and 5V is shown. If such a signal is integrated the average dc level will be 2.5V. This can be achieved by passing it through a filter with a cut-off lower than the signal's frequency. In

visual terms it can be considered as shown in (b). The upper half of the first half cycle fits neatly into the space provided by the second half cycle, producing a mean dc level of 2.5V. Note this cannot be achieved simply by using a reservoir capacitor because, assuming no load current, it would charge to the peak voltage of 5V. This has some similarity to the dc output of a mains power supply rectifier when followed by a capacity input filter and a choke input filter. The actual cut-off frequency of the filter is important and affects two matters, ripple and capture range. Using the mains filter analogy again, if the cut-off is not low enough—for instance, not enough inductance in the filter choke—there will be excessive ripple on the dc, and hum will result. In the case of the phase-locked-loop, the ripple will cause frequency modulation of the vco. Unfortunately a low cut-off frequency also means a narrow capture range, so we have two conflicting requirements of the filter, but we shall return to capture range and filter design later.

Now look at (c). The mark/space ratio is less than unity and the average dc level is lower. On an area comparison basis, more than half of the positive-going half-cycle would be needed to produce a mean dc level, and this would be less than 2.5V. Any further explanation to confirm that the dc output of a phase comparator and filter will vary as the phase difference between the two input signals varies should be unnecessary.

The author recently addressed a local radio club on matters arising from the earlier parts of this series and was able to demonstrate some methods of modifying the counting sequence of the basic binary counter. Perhaps one day it will be possible to distribute *Radio Communication* as a videotape, in the meantime words must suffice, but if readers who are still following this series (and the author hopes the majority are) would care to write on any points he would be glad to answer them in a subsequent article. Next month's will be the last regular part of this series, when the description of the phase-locked-loop frequency synthesizer will be completed. □

RAE COURSES 1976-7

The following list gives details of RAE courses which commenced in September but were received too late for inclusion in the lists published in the August and September issues.

December 1976 RAE. Listen to GB2RS on 10 October.

Bristol. Twyford House, High Street, Shirehampton. Includes morse instruction.

Chippenham. Chippenham Technical College, Cocklebury Road, Chippenham SN15 3QD. Details from G. C. Peck at the college, tel 0249 50501.

Coventry. Coventry Technical College, Butts, Coventry. Tuesdays, 7-9pm, commenced 14 September. Late enrolments possible until class full. Details from G8FFN, QTHR.

Croydon. Haling Manor High School, Kendra Hall Road, South Croydon. Tutor, P. L. A. Burton, G3ZPB. Thursdays, 7.30-9.30pm.

Edinburgh. Leith Nautical College, 59 Commercial Street, Leith. Mondays and Thursdays, 6.30-9pm, commenced 23 September. Includes morse. Late enrolment welcome. Fee £4.50. Details from the college, tel 031-554 4903.

Glasgow. Glasgow College of Nautical Studies, 21 Thistle Street, Glasgow C5. Tuesdays and Thursdays, 7-9.30pm, commenced 7 September. Fee £3, free to students under 18 as of 1 August.

London (Islington). Debeauvoir Evening Institute, Tottenham Road, Ballspond Road, London N1. Beginners Mondays and Wednesdays, advanced Tuesdays and Thursdays, commenced 20 September. Enrolment 13 September through to October. Details from senior instructor Fred Barnes, G3AGP, tel 01-864 5311 ext 2283 day, 01-361 9737 night.

LEARNING ABOUT LOGIC by P.J. Horwood, G3FRB*

Part 6. PLL frequency synthesizer (2)

WE have come a long way since Part 1 and the description of gates. This article adds more detail to the requirements of a frequency synthesizer and illustrates some of the techniques necessary in a practical design.

The dc amplifier and filter

Fig 42 shows a dc amplifier and filter added to the basic phase-locked loop. The amplifier is needed to increase the gain inside the loop, and improves the discrimination of the system. This may be compared to other feedback loops, eg the agc system of a receiver. In that case the greater the gain between the agc-controlled stage and the point where the signal is detected to form the agc control voltage, the smaller will be the change in signal output for a given change in signal input. Typically, a high-grade receiver's audio output will change by as little as 1dB for a change of as much as 100dB input. That represents about 20 per cent increase in output power for 100,000 times increase in signal voltage. In the case of a synthesizer one is aiming at a frequency stability within one or two hertz.

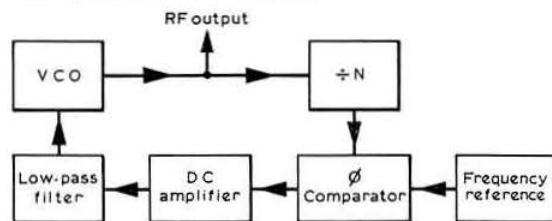


Fig 42.

The dc amplifier is required to amplify the square-wave output of the phase-comparator, which is integrated by the low-pass filter to form the varicap control voltage. As described in Part 5 the filter must have a cut-off frequency lower than the output frequency of the phase-comparator. While it is not intended to detail filter design here, the filter must not introduce significant phase-shift, for the comparator detects phase-shift to correct frequency, and since phase is the integral of frequency there is an unavoidable 90° phase-shift in the system. If the loop filter introduced another 90° shift the total would be 180°, changing the negative feedback to positive feedback, the result being instability or self-oscillation. The inbuilt 90° phase-shift of the system causes the loop gain to fall by 6dB per octave; this sets limits to the frequency range within which it will remain in lock.

Capture range and holding range

Capture range is defined as the maximum frequency difference between the unlocked vco and the desired locked frequency over which the system will pull into lock. For example, on switching on suppose a vco initially oscillated on 40MHz, the dc output of the comparator alters the capacity of the varicap so that the vco shifts to 50MHz

and the system locks. The capture range would be 10MHz. In practice the range would be limited by the bandwidth of the filter, and measures need to be taken to ensure that the vco is always within capture range despite relatively large changes in frequency which the vco may be required to make. Methods of doing so will be dealt with later.

Holding range is the maximum frequency range over which the system will correct vco error without lock being lost. Because the system is already in lock, the filter bandwidth is not a limiting factor. As has previously been explained, the filter is essential to remove the alternating component which would otherwise frequency modulate the vco. Furthermore the filter cut-off frequency is related to the reference frequency F_r , which also determines the size of the increments of frequency over which the synthesizer will change.

The filter design is always a compromise between the acceptable frequency modulation of the vco and the width of the capture range. It is possible, however, to use electronic switching of the bandwidth to reduce it by several hundred times after lock has been achieved. Fig 43 shows one possible method.

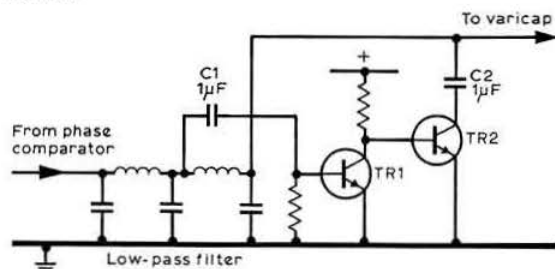


Fig 43.

When the system is out of lock there is present at the phase-comparator output a relatively low frequency signal produced by the vco sweeping about the lock frequency. This signal is tapped off the filter where the high-frequency output of the comparator is much attenuated, and via C1 causes TR1 to saturate. The collector of TR1 goes low, taking the base of TR2 with it, cutting it off. When lock occurs the low-frequency signal disappears, TR1 is now undriven and therefore cut off, and the collector goes high, taking TR2 base with it, and TR2 saturates, effectively connecting C2 in parallel with the filter output. Since C2 is large, the passband is much reduced and the vco is rendered less susceptible to spurious fm or jitter due to noise.

Preservation of capture range

A frequency synthesizer for the hf range is likely to require switching in 10MHz, 1MHz, 100kHz, 10kHz, 1kHz, and perhaps even smaller increments. For the purposes of explanation let us consider the three largest increments. When any one or a combination of them is altered the variable divider ratio will be so changed that the vco is likely to be outside the capture range. In the case of a 10MHz

* 14 Main Road, Hextable, Swanley, Kent.

change the vco coil may be switched by an additional wafer on the appropriate switch, thus shifting the vco to a new frequency inside the capture range. For smaller changes, eg 1MHz, an additional wafer on the 1MHz switch may be used to change the fixed capacitance in parallel with the vco coil, with the same result. Even smaller changes may be caused by switching a dc voltage to an additional varicap diode in the oscillatory circuit. This diode is outside the phase-locked loop; in other words it does not receive dc from the phase comparator and filter. Fig 44 illustrates all three methods.

Conclusion

The complete phase-locked-loop frequency synthesizer is a complex device; it has taken six articles to outline its operation and to give details of the problems and solutions involved in a practical design. Particularly in the last two articles much time has been spent on matters which are more analogue than digital, but the author hopes he has effectively shown how in modern communications digital techniques are closely married to analogue functions.

One reader has commented that he sees little point in understanding how groups of flip-flops can be made to divide by 10 when ICs such as the SN7490 can do it on one chip.

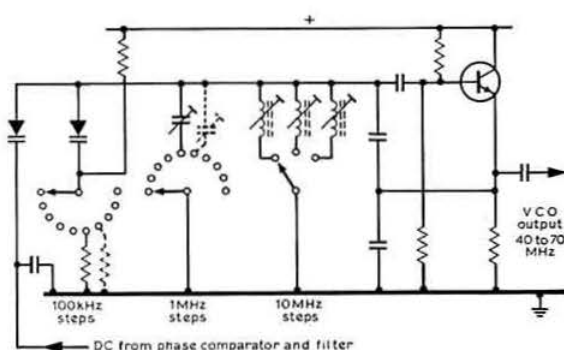


Fig 44.

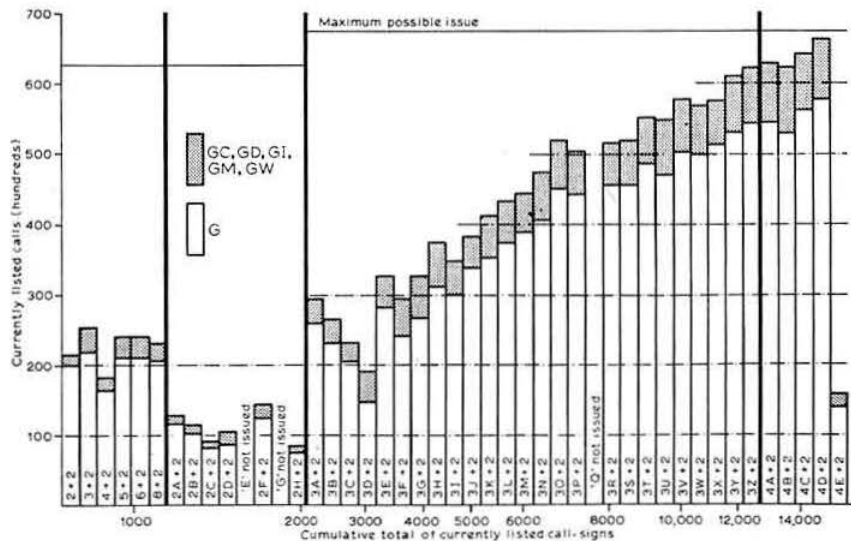
He has a point; no doubt a complete synthesizer will be available on an lsi chip sooner rather than later (and for those who may be tempted to say that complete phase-locked-loops are already available, that is not quite the same thing). But surely there is a limit to the black box approach; must many amateurs resign themselves to being perpetual appliance operators? □

A survey of Class A amateur licences

by A. O. SUTTON, G3MAJY*

THE histogram shows the distribution of some 15,000 Class A amateur licences from the earliest issue to G4EFZ (*RSGB Amateur Radio Call Book, 1976 Edition*). Pre-war calls from G2AA to G8ZK are shown in the first section—not necessarily in the order of issue—and number 1,375. Some 40 years after they were issued their ranks are sadly depleted; slightly less than a third now remain, not all of which are active. It is interesting to note that the letter "E" was never issued in this series, either as a first or second letter in the callsign. Perhaps the GPO thought that a possible G5EE, particularly on cw, might be a bit much! GC, GD, GI, GM and GW account for about 11 per cent of the total.

Next follow the pre-war artificial aerial licences—the G2 + 3 series, in which the letters "E" and "G" were not used; the former from both positions and the latter from the first letter position only. Comparatively few of this series remain listed—only about 20 per cent, inclusive of GM, GD, GW, etc; no doubt due to the second world war.



* "Westlands", Promenade, Leven, Fife KY8 4PH.

Possibly, too, some of these were allowed to lapse and helped to swell the post-war G3 + 3 boom, depicted in the third and largest section. Some 10,900 of these callsigns remain listed. This was also undoubtedly due to the war and its great demand for radio people of all sorts, with consequent training given to many who might otherwise never have had any interest in radio communication, amateur or otherwise. The author wonders, too, how many were hooked by that classic of its day *The RSGB Amateur Radio Handbook*, which sold for 2/6d! It was almost a textbook for the services in general. However, the immediate post-war era is now some 30 years back, and time has made inroads into the early G3As, Bs, etc. Indeed it is only from the issue of G3Js that the number of calls still issued equal about 50 per cent of the

Continued on p827